"High Efficiency Floating Junction GaAs Solar Cell for Space Applications"

Phase I Final Report
Contract # NAS3-27791

Submitted by:

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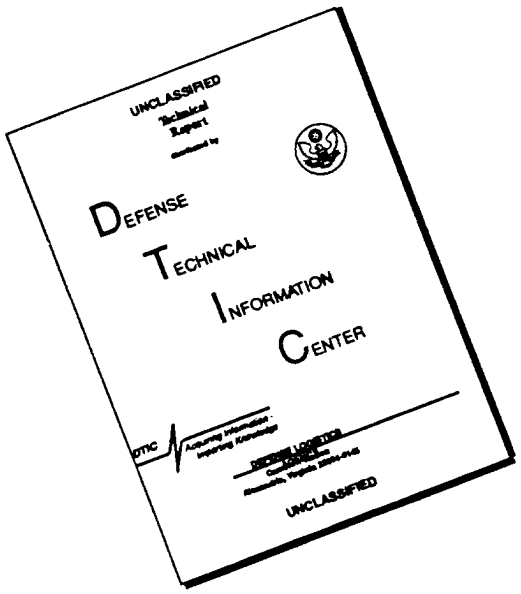

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1.0 PROJECT SUMMARY

AstroPower has demonstrated the feasibility of a lightweight, high efficiency GaAs solar cell that will have superior performance characteristics compared to conventional GaAs solar cells in the space environment. The solar cell design consists of a front floating junction coupled to a back collecting junction by the injection of minority carriers across a thin base. Performance benefits are enabled by incorporating an all back contact design with the electrostatic bonding technique and the use of multiple active junctions. The design of the floating junction GaAs solar cell is shown in Figure 1. By using the proper geometrical and electrical considerations, losses associated with grid shading and low energy radiation damage will be minimized. The Phase I effort demonstrated the objectives necessary to demonstrate proof of concept for a high efficiency floating junction GaAs solar cell. Continuation of process development in Phase II is anticipated to produce a radiation resistant solar cell with an efficiency greater than 21%. A summary of all the Phase I objectives and respective accomplishments follow.

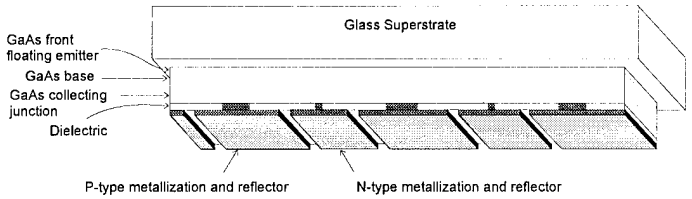
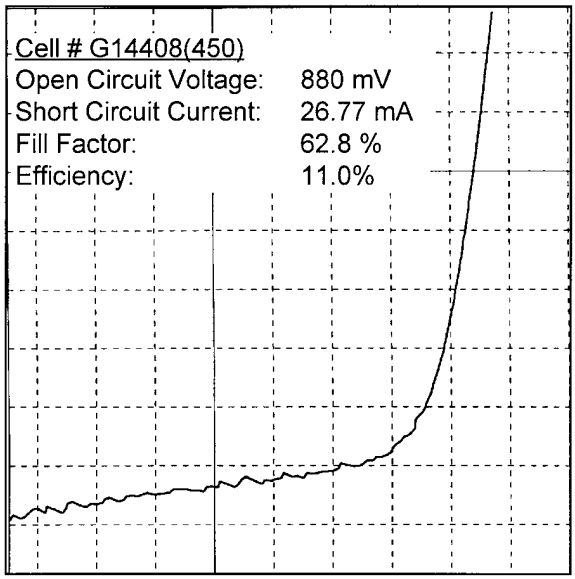


Figure 1. Floating junction GaAs solar cell.

- ❑ High Temperature Survivable Electrostatic Bonding
  - ✓ *Demonstrated electrostatic bonding to high temperature glass with 100% uniformity*
- ❑ High Temperature Processing Techniques
  - ✓ *Demonstrated 700 °C processing of thin, electrostatically bonded devices*
- ❑ Design Solar Cell Geometry
  - ✓ *Modeling with loss analysis predicts an efficiency of 21.9% for the current design*
- ❑ Single Step p/n Contact Metallization
  - ✓ *Demonstrated ohmic contact to p/n GaAs with Pd/In/Pd metallization*
- ❑ Prototype Device Fabrication
  - ✓ *11% (AM0), 1cm^2, no grid obscuration, 3 μm thick, floating junction solar cell*



The benefits of high temperature processing of electrostatically bonded GaAs to survivable glass superstrates can be applied to other solar cell designs such as tandem solar cells and high voltage concentrator cells. This device technology can be applied to electronic components operating at high temperature such as microwave circuitry and surface emitting lasers or operation in a thermally hostile environment by use of thin devices and a thermally conductive, high temperature substrate rather than a glass superstrate.

2.0 OVERVIEW OF PHASE I RESEARCH

2.1 Introduction

Gallium Arsenide (GaAs) is generally the material of choice when choosing a single material system for a space solar cell design. This is because GaAs has an optimal bandgap energy for conversion of the solar flux into electrical power. Gallium Arsenide epitaxial growth and processing techniques have matured to the point where production GaAs cells are routinely fabricated with beginning-of-life (BOL) efficiencies of 18-19%. However, increases in solar cell efficiencies are still desired and methods of improving them are rigorously explored. The use of high efficiency, multibandgap tandem solar cells as a production alternative is currently becoming a realization. These cells are predicted to have BOL efficiencies of over 23% [CHIANG, ET AL, 1995]. However, due to the extreme sensitivity of these tandem solar cells to such issues as current matching, their performance in a harsh space environment still remains a concern. The tandem cell's performance will dramatically decrease when the cell is no longer current matched. Loss of current matching is predicted for a multibandgap cell, since the multiple alloy compositions will display different damage coefficients in a given radiation environment. AstroPower's solution to this problem involves a multijunction design that has no current matching requirements. The cell design takes advantage of the well understood GaAs/AlGaAs system, yet combines many of the benefits of a multijunction solar cell (i.e. increased current collection) with a design that yields a potential radiation resistance greater than both conventional GaAs solar cells and multibandgap tandems.

The floating junction GaAs solar cell is designed to achieve AM0 efficiencies approaching 21.9 %, while providing a high degree of radiation resistance for high end-of-life (EOL) efficiencies. A radiation resistant solar cell is predicted, using the floating junction design, due to the minimal transit lengths necessary for diffusing carriers to reach a junction. Short circuit current will be maintained because of the minimal distances required for photogenerated carriers to diffuse to either the front or back junction. Open circuit voltage will be maintained when a properly designed floating emitter suppresses minority carrier recombination in the vicinity of the collecting junction. Other advantages of this solar cell design include:

- High specific power
- Electrostatic bonding eliminates degradation associated with adhesive bonded cells
- Zero grid shading
- Light trapping
- Coplanar back contacts

2.2 Theory of Operation

Figure 2 illustrates the device layer compositions and thicknesses of the floating junction GaAs solar cell. For the Phase I effort, all material was grown by liquid phase epitaxy (LPE), however, any growth technique would be applicable to this design. The collecting junction is diffused through the back of the solar cell after the substrate is chemically removed. The notation used in the remainder of the report will refer to the active regions of the solar cell as the emitter, the base and the collector, with the emitter being the open circuited layer at the top of the cell.

Device operation is as follows: carriers generated by light absorbed near the collecting junction will diffuse and be collected by the collecting junction. It is the collecting junction that is actually connected electrically to the load. Photogenerated carriers in the vicinity of the floating junction will diffuse and be collected by the floating junction. However, since the front junction is open circuited, no net current may flow across this junction. To retain open circuit voltage conditions, a current equal and opposite to the photogenerated current in this region must flow across the junction. This current is the injection (diffusion) current, which is characterized by the injection of minority carriers into either side of the junction. Injection of carriers from the emitter into the base is the ideal case, since these carriers may be collected by the collecting junction, provided the carriers do not recombine during transport across the base. Injection of carriers from the base into the emitter will result in a loss in short circuit current, since they will recombine in the disconnected emitter. The nature of the injection mechanism is dependent on the energy barrier and carrier diffusivities near the junction.

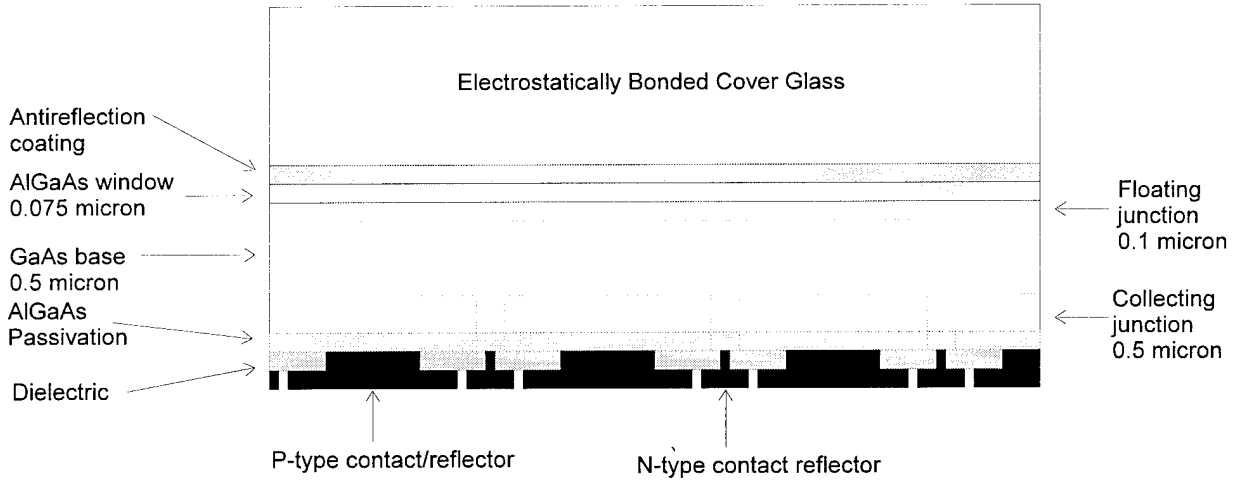


Figure 2. Ultra-thin floating junction GaAs solar cell.

Figure 3 illustrates four cases where light is absorbed on either side of the floating junction, with a p-type emitter. The desired current flow is such that the diffusion current consists only of injection of holes into the base. Cases 1 and 2 illustrate carrier generation in the emitter. Case 1 consists of an electron drifting across the junction into the base and a hole injected into the base. Case 2 consists of an electron drifting across the junction which is subsequently reinjected back into the emitter, resulting in a short circuit current loss. Cases 3 and 4 illustrate analogous current flows for generation in the base region. Note that in all four cases the net current across

the floating junction is zero. Fortunately, the injection mechanism is easily controlled by introducing a small bandgap discontinuity between the two layers. The use of a widegap floating emitter will suppress carrier injection into the emitter region [KROEMER, 1982]. This is discussed in Section 4.3.

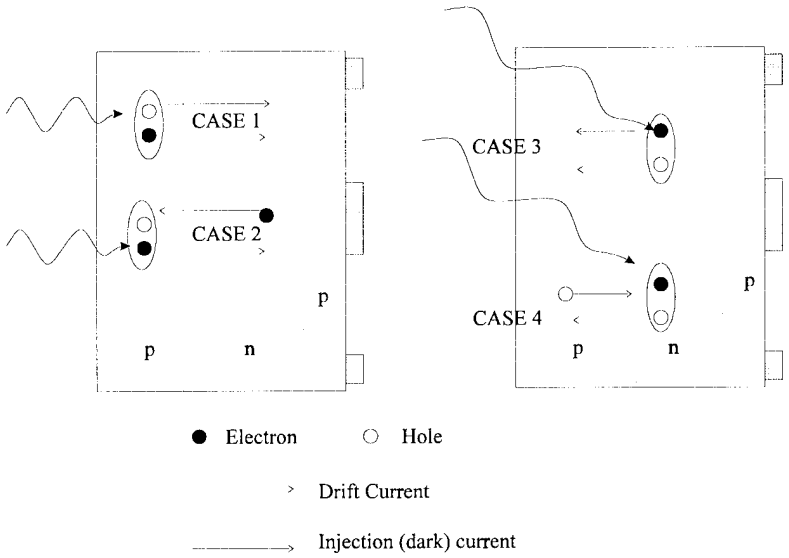


Figure 3. *Illustration of holes injected across base into collecting junction where they will be collected by the collecting junction (case 1 and 4) and electrons injected into emitter where they will recombine, resulting in a short circuit current loss (case 2 and 3).*

A front floating junction, whose diffusion current is dominated by minority carrier injection into the base, will also maintain a high open circuit voltage at the collecting junction. The open circuit voltage effect is best expressed in this discussion in terms of J_o, the saturation current density. The open circuit voltage is inversely proportional to the natural logarithm of J_o [GREEN, 1992]. Thus, a high open circuit voltage requires a low J_o. The saturation current is proportional to the slope of the minority carrier distribution at the junction edge under forward bias. The slope is related to the recombination of the injected minority carriers in the bulk of the semiconductor. The potential barrier and the injection of carriers from the front floating junction will tend to decrease the slope of the minority carrier distribution in the base, and thus decrease the saturation current densisty of the collecting junction. The effect of reducing the slope of the minority carrier distribution due to the potential barrier "minority carrier mirror" and injection from the front junction is shown in Figure 4. Points x_o and x_o+x_b represent the edges of the floating junction and the collecting junction, respectively. The dotted lines indicate the minority carrier distribution if each junction were operating independently.

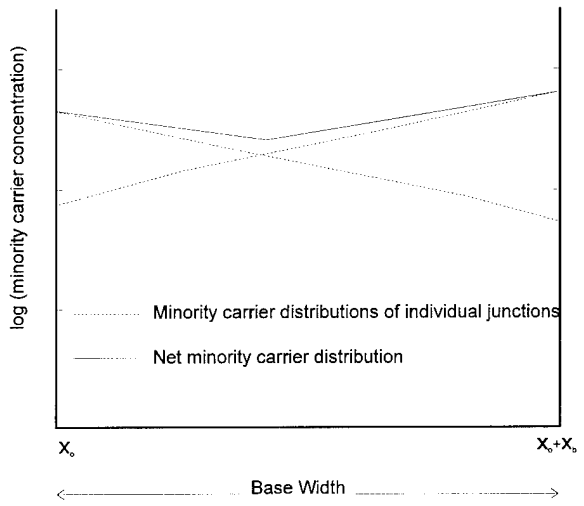


Figure 4. Effect of front floating junction on slope of minority carrier distribution.

Similar arguments for use of a floating junction structure can be found for silicon solar cells [GHANNAM, 1991 AND HONSPERG, 1994]. The silicon design places the floating junction at the back of the solar cell to effectively passivate the back surface of the device. The passivation is predicted to yield higher open circuit voltages compared to devices implementing a back surface field or thermal oxide. GHANNAM predicts the reduction in dark diode current and corresponding open circuit voltage increase using Ebers-Moll analysis for an n-p-n bipolar junction transistor as:

$$I_{o,t} = \alpha_n I_{eo}\left(\frac{1}{\alpha_n} - \alpha_I\right) \qquad \Delta V_{oc} = (0.026)\left(\ln\frac{I_o}{I_{o,t}}\right)$$

where $I_{o,t}$ is the reduced reverse saturation current of the connected junction with the floating junction at open circuit conditions, α_n is the normal mode base current gain of the transistor, α_I is the inverse mode common base current gain, I_{eo} is the emitter-base saturation current and I_o is the reverse saturation current of a standard n^+p silicon solar cell with a back surface field. The gain in open circuit voltage for a floating junction silicon cell is predicted to be between 25 and 50mV higher than the gains obtained with a good to moderate quality oxide.

The benefit of leaving the emitter disconnected at the front floating junction becomes apparent when considering the emitter sheet resistance of a conventional solar cell. Figure 5 illustrates the simplified current conduction paths followed in a conventional solar cell design. A fundamental conflict exists for the conventional solar cell design because of the contribution of emitter sheet resistance to the series resistance losses. The sheet resistance must not introduce a significant voltage drop when conducting the lateral emitter current to the grid lines. This is accomplished by heavy doping and/or a deep emitter. While this method will suppress series resistance losses in the emitter, it may degrade the efficient collection of high energy light in a space environment. Because GaAs has such a high absorption coefficient, a significant fraction of usable light is absorbed near the surface. This requires that the emitter thickness be smaller than a minority carrier diffusion length throughout the lifetime of the device. A conventional solar cell design attempts to make the emitter as shallow as possible, however the depth will

always be limited by sheet resistance considerations. The floating junction GaAs solar cell does not need to take emitter sheet resistance into account because the floating junction is disconnected. No lateral current flow exists as it does for the conventional cell shown in Figure 5. The floating emitter depth can be designed for any ratio of diffusion length to emitter thickness. Thus, the floating junction GaAs solar cell will retain the high energy photon response in a harsh radiation environment.

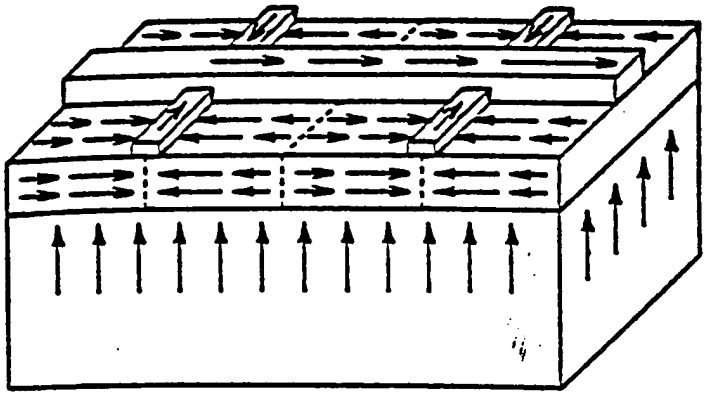


Figure 5. Simplified model of current flow in a conventional solar cell.

Another benefit of the floating junction GaAs solar cell design is that there are no front grids to obscure light from entering the device. Therefore, nearly 100% of the available light can be utilized. By properly designing the collecting junction, there will be negligible short circuit current losses associated with geometrical losses (i.e. recombination of diffusing carriers due to length of transit). This is discussed in more detail in Section 4.3.

2.3 Electrostatic Bonding

When compared to adhesive bonding, the electrostatic bonding method of attaching space solar cells to glass covers has several advantages. First, there is no darkening effect such as that which occurs with adhesives after extended exposure to UV light, and there is no degradation of the bond because it is chemical and permanent. Second, the maximum power to weight ratios can be attained since no additional material is used to form the bond, and third, the survivability of an adhesive bonded ultra-thin solar cell is questionable if it is exposed to a temperature moderately above or below that temperature at which the adhesive layer was cured (typically 150 °C).

The electrostatic bonding process is well documented [WHITE, ET AL (1988)] and is generally well known. It is a permanent, chemical/ionic bond that occurs between glass and many types of metals, semiconductors and insulators at elevated temperatures and pressures upon the application of a several hundred volt potential across the surfaces to be bonded. Figure 6 is a schematic representation of the electrostatic bonding process.

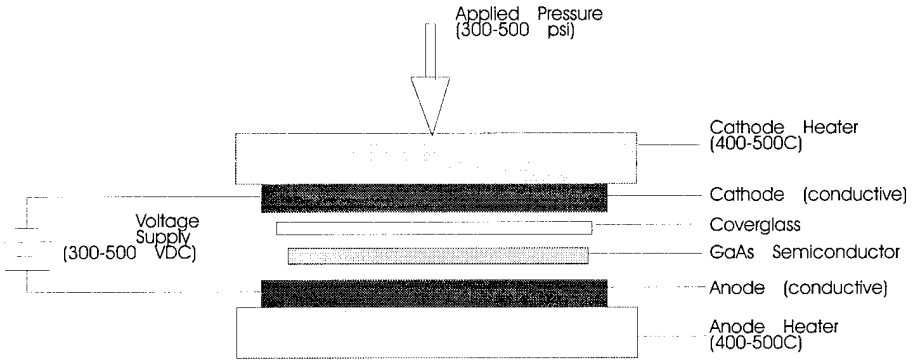


Figure 6. Schematic representation of the electrostatic bonding procedure.

Critical to the success of the floating junction GaAs solar cell is the availability of a high temperature glass whose coefficient of thermal expansion (CTE) matches that of GaAs over the process's temperature range. The ultra-thin GaAs/glass laminate must endure a wide range of processing temperatures: from room temperature processing to diffusion temperatures. Currently, a space qualified, commercially available glass (Pilkington-CMG) only matches the CTE requirements up to the glass's softening point (approximately 350°C). This glass will not survive the temperatures encountered during processing of the solar cell. For this program, a CTE matched glass was obtained with a softening point of 890 °C. This temperature is well above all temperatures encountered during processing. Details on the procedure for electrostatic bonding to high temperature glass and the subsequent high temperature processing can be found in Sections 4.1 and 4.2, respectively.

2.4 Light Trapping

The floating junction GaAs design will incorporate light-trapping to improve performance during the solar cell's lifetime. The benefits of light-trapping in GaAs can be realized by increased optical absorption, collection efficiency and photon recycling. The first two benefits are due to the increased optical path length and decreased base thickness of the solar cell. Photon recycling occurs when a photon is emitted during a radiative recombination process. This photon is optically confined in the vicinity of the collecting junction and is subsequently reabsorbed, creating an electron-hole pair. Photon recycling increases the effective minority carrier lifetime in the material. All three of these features lead to increased open circuit voltages and short circuit currents.

The floating junction GaAs solar cell incorporates light-trapping by depositing a reflector on the back of the solar cell. The current design incorporates a silver reflector deposited over a transparent dielectric layer as shown in Figure 1. The benefit of this methodology is that the reflector acts as a low resistance conductor. The conductor eliminates the need for electroplating the contacts, thus eliminating several process steps. Alternative reflectors include the use of a Bragg reflector, consisting of alternating layers of silicon and silicon dioxide deposited by the PECVD process. Both methods result in similar reflectivities for the wavelengths of interest.

3.0 PHASE I WORKPLAN

The broad objective of the Phase I program was to demonstrate the feasibility of the high efficiency GaAs floating junction structure. Incorporation of the electrostatic bonding technology into a high temperature processing sequence was necessary to accomplish this goal. Optimization of the device structure was accomplished with computer aided modeling of the transport properties of the device. A prototype floating junction GaAs solar cell was fabricated and characterized using conventional solar cell and semiconductor analysis.

3.1 Phase I Specific Objectives

Task 1. Integrate the technique for high temperature survivable electrostatic bonding of GaAs to glass superstrates.

Task 2. Develop high temperature processing techniques for ultra-thin GaAs/glass laminates.

Task 3. Design the geometry necessary to achieve maximum current collection while keeping manufacturing costs low.

Task 4. Demonstrate the technology for accomplishing ohmic contact to n- and p- type AlGaAs in a single monolithic process.

Task 5. Demonstrate the feasibility of the floating junction solar cell by building a prototype device and characterizing the performance.

3.2 Phase I Questions

1. Is a 100% transparent grid design attainable using current patterning and metallization technologies? Is it compatible with the high temperature process?
2. Is the monolithic contacting sequence compatible with the ultra-thin device layers of the floating junction solar cell?
3. Will the high temperature processing steps affect the electrostatically bonded device or alter the conductivity of the device layers?
4. What are the benefits of the floating junction solar cell over conventional gallium arsenide solar cells?
5. Will the PECVD Bragg reflector be compatible with a low cost interconnection scheme? How will its performance compare to a conventional metallic reflector?

3.3 Work Schedule

Task		Month					
1	Integrate high temperature survivable electrostatic bonding technology	X	X	X			
2	Develop high temperature processing techniques	X	X	X	X	X	
3	Design optimal geometry			X	X	X	
4	Develop monolithic metallization			X	X	X	
5a	Characterize performance of devices				X	X	X
5b	Determine feasibility						X
6	Draft Final Report						X

3.4 Summary of Results

A summary of the results accomplished during the Phase I effort is listed below:

- Demonstrated an 11% efficient floating junction solar cell with a GaAs thickness of 3 μm.
- Obtained a glass compatible with thin GaAs laminates up to 700 °C.
- Demonstrated electrostatic bonding to high temperature glass with 100% uniformity.
- Demonstrated high temperature (700 °C) processing of thin, electrostatically bonded devices.
- Designed the solar cell geometry for a typical space mission.
- Modeled solar cell performance.
- Demonstrated ohmic contact to n- and p-type AlGaAs.

The Phase I effort demonstrated the high temperature processing of 3 μm thick, electrostatically bonded, GaAs solar cells. A prototype floating junction solar cell was fabricated with an AM0 efficiency of 11%. Further improvements in the processing of the floating junction GaAs solar cells are expected to yield efficiencies approaching 21%. The floating junction design also offers improvements over conventional GaAs solar cells when considering EOL efficiencies in the space environment due to a reduced dependence on surface recombination velocities. This effect will be explained in detail in Section 4.3. The design is capable of obtaining the highest short circuit currents possible, by implementing a no grid obscuration design coupled with light trapping. Light trapping may be achieved by either a metal reflector or with a PECVD SiO_2/Si Bragg reflector. Both offer high reflectivity for the wavelengths of interest, however the metal reflector offers the additional benefit of conducting current for the solar cell. This benefit eliminates several process steps and thus is the method of choice when considering solar cell manufacturing.

4.0 PHASE I RESULTS

4.1 Task 1. Integrate the technique for high temperature survivable electrostatic bonding.

Critical to the success of the program was the development of a glass formulation whose coefficient of thermal expansion (CTE) matched the CTE of GaAs over a wide range of temperatures. Because the solar cell design calls for several high temperature process steps for the ultra-thin GaAs/glass laminates, many CTE matched glasses, such as Pilkington CMG space glass, will not survive the fabrication process due to their low softening point. The solution lies in the development of a thermally matched glass whose softening point is higher than the highest temperatures encountered during the solar cell processing sequence. This includes the diffusion, contact alloy, PECVD deposition and electrostatic bonding process temperatures.

A high temperature survivable glass formulation has been developed with Sem-Com Co., Inc. (formula E10050) to match the CTE of gallium arsenide up to the strain point of the glass (674°C). The glass has a softening point of 890 °C and a CTE of 6.0×10^{-6}/K. Uniform electrostatic bonding of this glass to GaAs was repeatably demonstrated with no physical degradation of either the glass or the semiconductor material. A short description of the electrostatic bonding process can be found in Section 2.3.

There are two critical parameters that directly affect the quality of the electrostatic bond between GaAs and the high temperature glass. These parameters are the anti-reflection coating and the temperature of the GaAs/glass interface during the electrostatic bonding procedure.

AstroPower has found that electrostatically bonding GaAs directly to glass results in incomplete bond formation and voids. This problem is alleviated by depositing an intermediate dielectric layer at the surface of the GaAs prior to bonding. The quality of both the bond and the anti-reflection coating is dependent on the composition of this dielectric layer. Several compositions were investigated and the results are shown in Table 1.

Table 1. Summary of dielectrics explored for electrostatic bonding GaAs to glass.

Dielectric Composition	Deposition Method	Thickness	Results
SiO_2	PECVD	60 nm	Poor Bond
Si_3N_4	PECVD	60 nm	Poor Bond
Al_2O_3	E-beam evaporation	60 nm	Poor Bond
$Si_xO_yN_z$	PECVD	60 nm	Excellent Bond

The use of materials such as silicon nitride, silicon dioxide and evaporated aluminum oxide as interface layers results in a significant area of incomplete bond formation at the glass/semiconductor interface. A photograph of an electrostatically bonded sample with an evaporated aluminum oxide interface layer is shown in Figure 7. Approximately 5% of the total area was successfully bonded, with the remaining area being characterized as air voids between the GaAs and the glass.

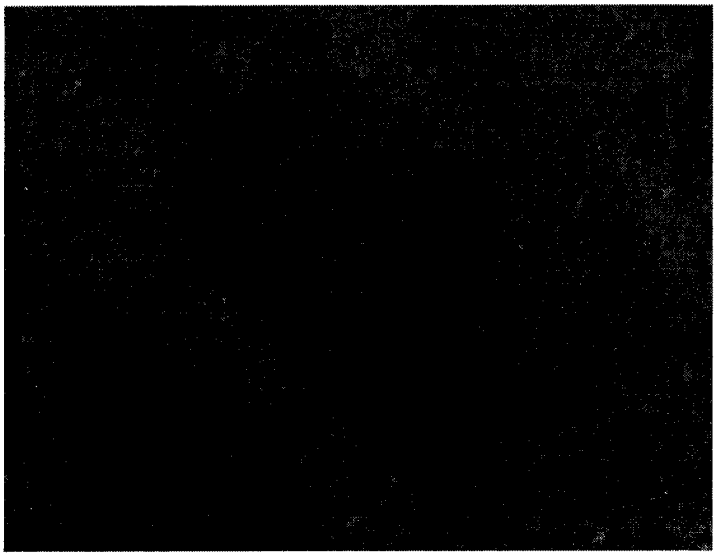


Figure 7. *1000X photograph showing an unsuccessful electrostatic bond of GaAs to glass using Al_2O_3 as an interface layer.*

A successful void-free electrostatic bond to GaAs occurs when a thin coating of silicon-oxynitride ($Si_xO_yN_z$) is applied to the front surface of the semiconductor. The refractive index of the $Si_xO_yN_z$ (approximately 2.2 for visible wavelengths) also minimizes reflection at the interface. Four ultra-thin floating junction devices with uniform electrostatic bonds are pictured in Figure 8. All devices had approximately 60 nm of PECVD $Si_xO_yN_z$ deposited on the front surface of the GaAs prior to bonding.

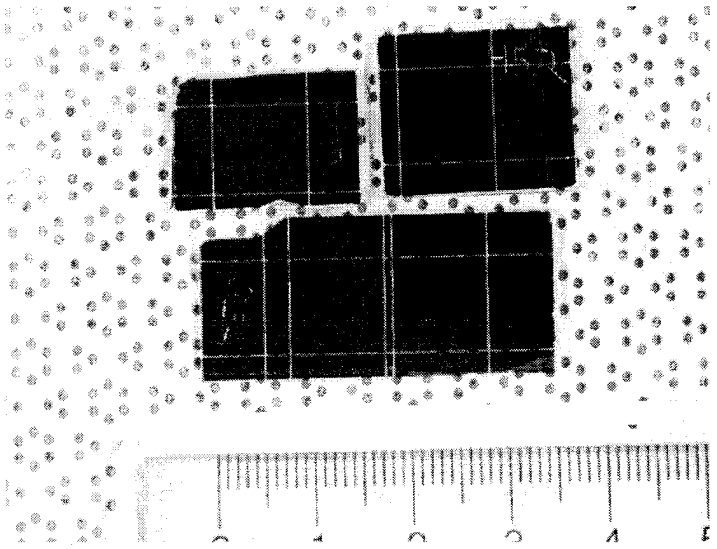


Figure 8. *Photograph showing successful electrostatic bonding of GaAs to glass using $Si_xO_yN_z$ as an interface layer. Four 1x1cm^2 floating junction solar cells are depicted.*

The second critical parameter for successful electrostatic bonding to GaAs is the temperature used during bond formation. The temperature must be high enough to activate mobile carriers in the glass so that charge transfer occurs; this corresponds to the strain point of

the glass (674 °C). For the high temperature glass formulation (E10050) it has been found that the 630-650°C range is the minimum temperature needed to achieve a uniform bond. No bonding occurs for temperatures below 600°C. This is true for formulations with sodium concentrations ranging from 0% to 2%. The addition of the mobile ion, sodium does not affect the minimum temperature necessary for successful bonding. The parameters used for electrostatic bonding of GaAs to the high temperature glass are listed in Table 2.

Table 2. High temperature glass/GaAs electrostatic bonding parameters.

Bond Area	Temperature	Applied Pressure	Time	Applied Voltage
1-4 cm^2	650°C	1500 psi	2-4 minutes	$750V_{DC}$

Uniform electrostatic bonds were obtained between GaAs and the high temperature glass. These laminates survived all subsequent processing steps with no warping or any other physical defects. Details on the processing of the GaAs/glass laminate will be discussed in Section 4.2.

4.2 Task 2. Develop high-temperature processing techniques for ultra-thin floating junction/GaAs laminates.

Processing of the floating junction GaAs device requires several steps which may induce stress to the GaAs/glass laminate. A general process sequence was devised, with revisions being made as devices were fabricated and tested. A summary of the process steps used to achieve an 11% efficient floating junction structure is listed below and depicted in Figure 9.

Floating Junction GaAs Process Sequence

1. Grow active device layers on GaAs substrate.
2. Deposit a 60 nm $Si_xO_yN_z$ anti-reflection coating on the front surface of the epi-layers (Figure 9a).
3. Electrostatically bond the solar cell to the high temperature glass superstrate (Figure 9b).
4. Remove the GaAs substrate in an agitated hydrogen peroxide:ammonia hydroxide (20:1) solution (Figure 9c).
5. Deposit a 500 nm $Si_xO_yN_z$ diffusion barrier on the back of the thin solar cell. Pattern diffusion vias using standard photolithography and plasma etching techniques (Figure 9d).
6. Diffuse p-type collecting junction at 700 °C in open tube zinc diffusion chamber (Figure 9e).
7. Pattern and deposit n-type (base) and p-type (collector) metallization (Figure 9f).
8. Deposit and pattern a dielectric layer for insulation of the n-type and p-type conductors (Figure 9g).
9. Pattern and deposit metallization for the back conductors/reflectors using 300 nm of evaporated silver (Figure 9g).
10. Test.

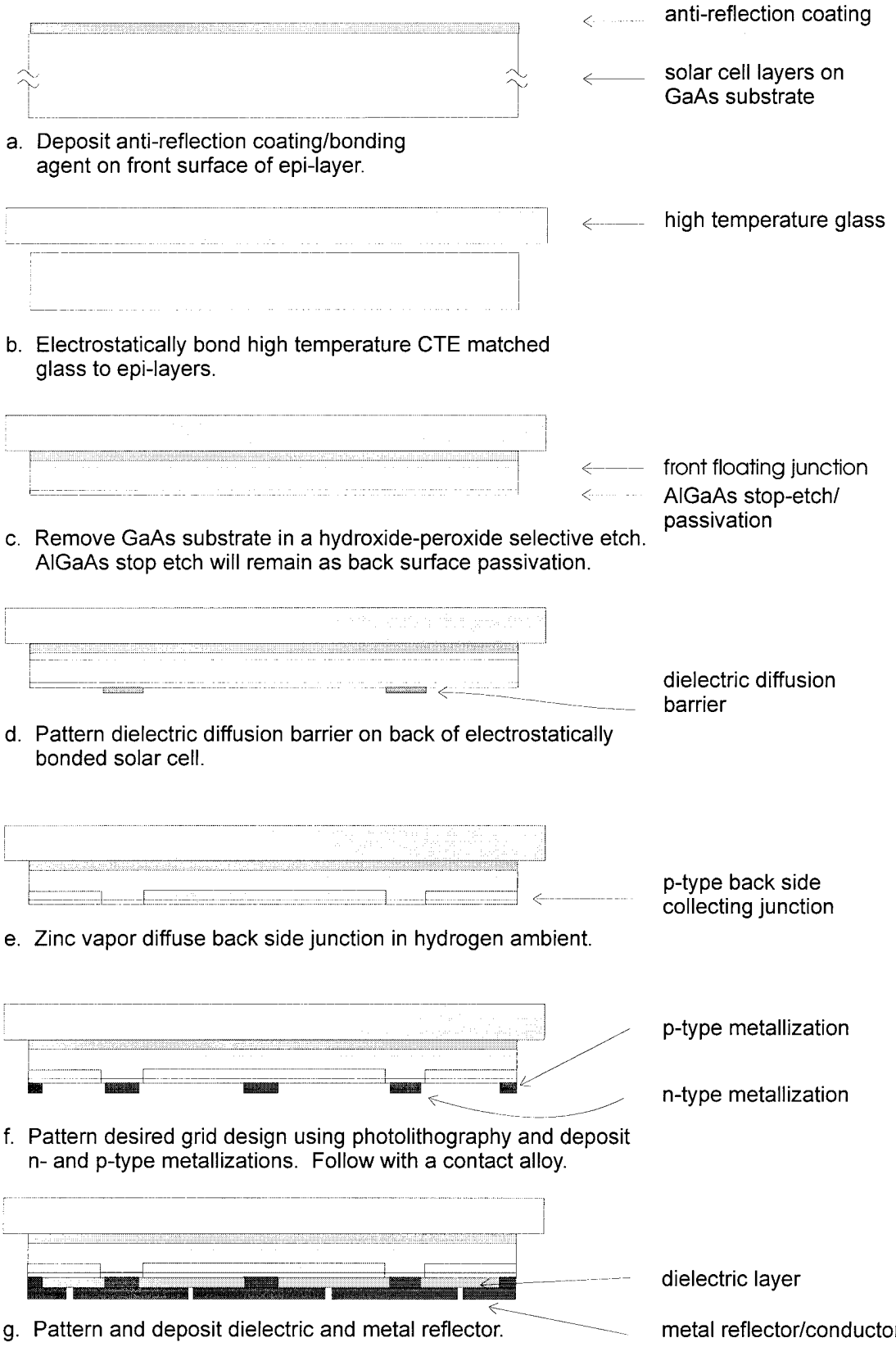


Figure 9. Process sequence for floating junction GaAs solar cell.

The active layers are grown by LPE. The base carrier concentration is $N_D = 2x10^{17}$ cm^{-3} and the emitter is diffused with beryllium during the isothermal growth of the thin $Al_{0.9}Ga_{0.1}As$ passivation layer [KORDOS, ET AL, 1979]. The cell is electrostatically bonded to the high temperature glass, as described in Section 4.1. After the electrostatic bonding procedure, there are several critical steps that must not degrade the device performance and/or the structural integrity of the solar cell. These include the collector diffusion, the contact alloy and the PECVD dielectric deposition. These high temperature steps may induce either compressive or tensile strain on the active device. Also, redistribution of the dopant atoms may occur during the diffusion, resulting in a non-optimal doping profile. All of these effects must be avoided for a stable, high performance solar cell.

Diffusion

The back collecting junction is formed via open tube diffusion of zinc in a purified hydrogen environment. A graphite boat is used which allows the sample to be placed under a zinc overpressure region. The diffusion time and temperature determine the depth of the back collecting junction. The requirements for a successful diffusion are:

1) The solar cell must not experience physical degradation, such as warping, delamination or breakage.
2) The diffusion must compensate the n-type base so that a p-n junction may be formed.
3) The diffusion barrier must withstand the thermal cycle.

Various diffusion times and temperatures were investigated. At a diffusion temperature of 700 °C, a thin, highly doped p-region forms at the back of the solar cell. The diffusion profile for a 120 minute open tube zinc diffusion performed at 700 °C is shown in Figure 10. The p-type layer was diffused into an n-type (Si: $1x10^{18}$ cm^{-3}) substrate and was profiled by an electrochemical capacitance-voltage measurement performed at BioRad Semiconductor in Mountain View, California. The depth of diffusion for this sample is approximately 1 μm with a peak concentration of $1.5x10^{19}$ cm^{-3}. The corresponding sheet resistance of this layer is 200 ohms per square.

The diffusion at 700 °C caused no visible damage or warping to the glass, the solar cell or the diffusion barrier. The cell remained flat after the 30 minutes required for diffusion of the collecting junction, indicating that the interface did not experience thermal stress/strain. Diffusions at higher temperatures (750 °C) were performed which resulted in warping of the GaAs/glass laminate. Temperatures exceeding the strain point of the glass result in a nonlinear CTE for the glass and thus is no longer matched to the CTE of the GaAs.

No redistribution of beryllium acceptor atoms in the floating junction was observed after the high temperature processes. This was verified by optical inspection of a cleaved sample using a standard type-sensitive etch. Beryllium is a slow diffusing impurity for all except the highest beryllium concentrations [SCHUBERT, 1993].

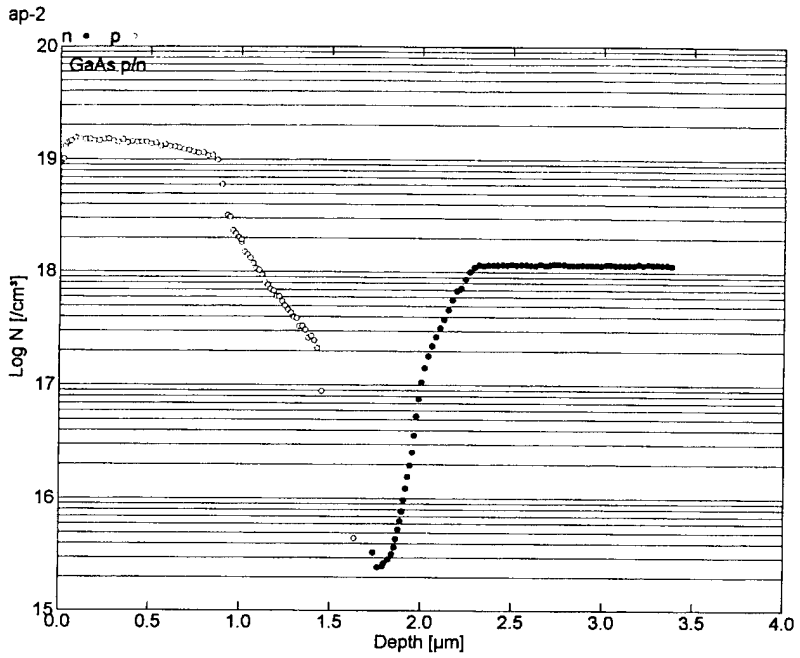


Figure 10. Electro-chemical etch profile for 700 °C open tube zinc diffusion.

Contact Alloy and PECVD Deposition

Contact alloy and PECVD deposition of dielectric layers are standard solar cell processing techniques that range in temperature from 300 °C to 500 °C and are characterized by rapid heating and cooling of the solar cell. Processing of the thin, electrostatically bonded GaAs solar cell requires two PECVD depositions at 300 °C and one contact alloy at 450 °C. Floating junction GaAs solar cells fabricated using the process presented in Figure 9 suffered no adverse effects during the PECVD deposition and contact alloy steps.

4.3 Task 3. Design the geometry necessary to achieve optimal photogeneration and current collection.

The layer compositions and thicknesses for the floating junction GaAs solar cell were optimized using a one dimensional analysis, followed by a three dimensional analysis of the resistive losses present in the solar cell. The one dimensional analysis of Poisson's equation and the current continuity equation was accomplished using PC-1D Version 3.0, a software program developed at Sandia National Laboratory [BASORE, 1991]. The modeling of the floating junction GaAs device, using PC-1D, indicated the doping densities, alloy compositions and layer thicknesses necessary to achieve a high efficiency solar cell. Using the parameters derived with this software package, a three dimensional model was set up to predict the losses associated with finite geometries (i.e. I^2R losses associated with current collected by the grid).

PC-1D Modeling

The numerical method of PC-1D uses the two-carrier, semi-classical, semiconductor transport equations derived from the Boltzman transport equation [BASORE, 1991]. The program requires the following inputs: layer thicknesses and compositions, doping levels, circuit parameters, temperature, and boundary conditions such as surface and interface recombination

velocities. All of the above parameters may be varied and simulated so that the illuminated current-voltage characteristics may be optimized.

Table 3 lists the input parameters for modeling a high efficiency floating junction GaAs solar cell. There are several variations of the design which will produce similar BOL results. However, the particular parameters chosen in Table 3 provide the potential for the highest end-of-life (EOL) efficiencies in a harsh radiation environment. Table 4 summarizes the results.

Table 3. PC-1D parameters for floating junction GaAs solar cell

Symbol	Description	Value	Units
N_{Ae}	Acceptor concentration in floating emitter	$1x10^{18}$	cm^{-3}
N_{Db}	Donor concentration in base	$5x10^{16}$	cm^{-3}
N_{Ac}	Acceptor concentration in collector	$1x10^{18}$	cm^{-3}
t_e	Thickness of $Al_{0.1}Ga_{0.9}As$ floating emitter	0.1	μm
t_b	Thickness of GaAs base	0.5	μm
t_c	Thickness of GaAs collector	1.5	μm
S_f	Effective front surface recombination velocity	10^4	cm/s
S_b	Effective back surface recombination velocity	10^4	cm/s
R_f	Front surface reflection	4	%
R_b	Back surface reflection due to light trapping	90	%
ϕ	Incident AM0 light intensity	1350	W/m^2
T	Cell temperature	25	°C

Table 4. Results of PC-1D modeling.

open circuit voltage (Volts)	short circuit current density ($mA/cm^{2)}$	fill factor (%)	AM0, 1X efficiency (%)
1.012	35.03	85.6	22.5

Figure 11 displays how the performance of the modeled floating junction GaAs solar cell is relatively insensitive to changes in front surface recombination velocity when compared to conventional GaAs solar cells with similar BOL characteristics. Note that the floating junction consists of a wide-gap emitter (ΔE_g = 0.08 eV), similar to the design of a heterojunction bipolar transistor [KROEMER, 1982]. The conventional GaAs solar cell structure consists of a 0.5 μm emitter ($N_A = 2x10^{18}$ cm^{-3}) and a 5 μm base ($N_D = 2x10^{17}$ cm^{-3}) with a passivated back surface reflector. The initial surface recombination velocity represents typically reported values for a GaAs surface passivated with a thin AlGaAs window layer. The increase in front surface recombination velocity could represent one of the adverse effects encountered in a harsh radiation environment.

The three graphs in Figure 11 compare the performance of a floating junction and a conventional GaAs solar cell as a function of front surface recombination velocity. The performance of the front floating junction is relatively independent of the quality of the front

surface in comparison to the conventional GaAs solar cell. The open circuit voltage and short circuit current density of the floating junction structure remain high for front surface recombination velocities of $1x10^7$ cm/s. This performance enhancement can be attributed to the extremely thin emitter and the offset in the conduction band energy due to the slight variation in the alloy composition between the emitter and base.

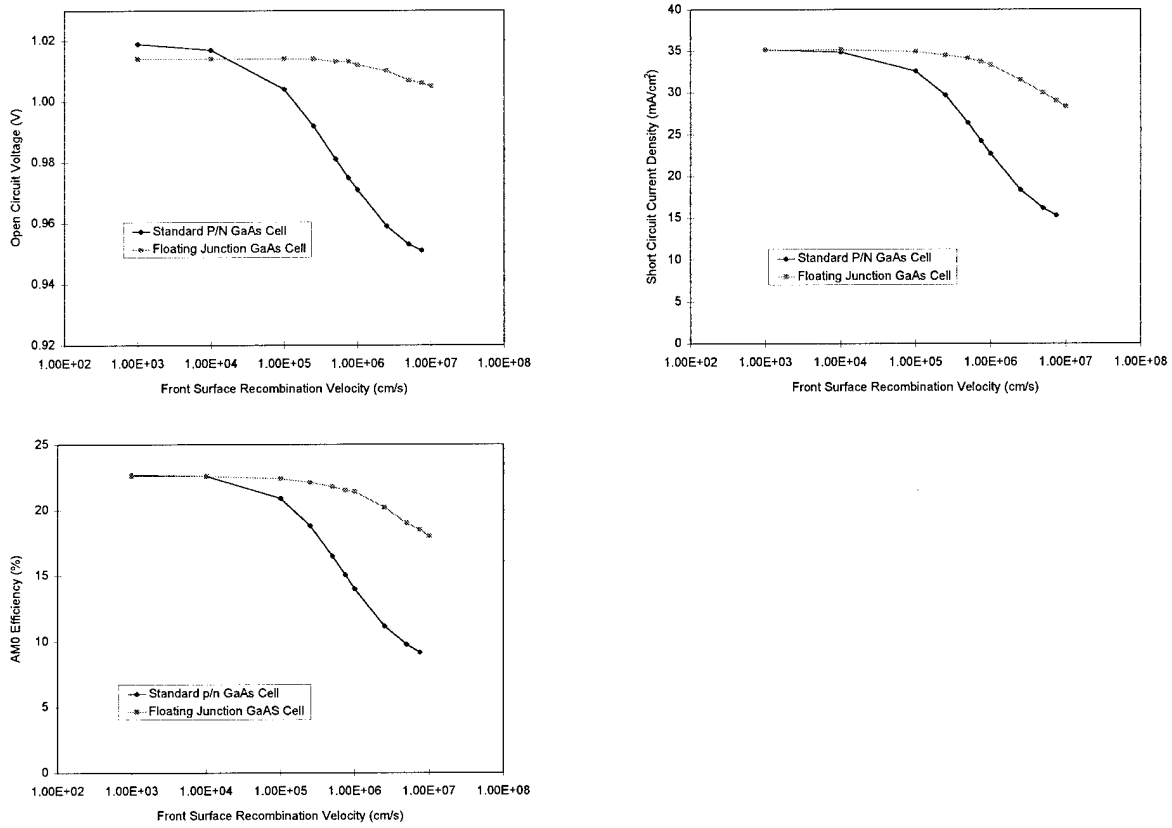


Figure 11. PC-1D Comparison of open circuit voltage, short circuit current and efficiency as a function of surface recombination velocity.

The thin emitter (100 nm) is suitable for this design because there is no net current collection at the front floating junction. Thus, there is no lateral current flow in this region as in a conventional solar cell, and the sheet resistance of the layer has no effect on the cell's series resistance. This allows a greater fraction of the light to generate carriers in the base and collector, while the front heterojunction suppresses injection current into the thin emitter due to the conduction band offset. The result is a lower net surface recombination current density than would be seen in a conventional solar cell. The floating junction GaAs cell with a wide gap emitter maintains a high short circuit current for even the most poorly passivated surface.

A high open circuit voltage, relative to the conventional design, is maintained in the front floating junction structure due to the $Al_{0.1}Ga_{0.9}As/GaAs$ conduction band offset at the front floating junction. Because the front floating junction and the back collecting junction are closely coupled due to their proximity, it is important that the front floating junction does not adversely affect the electrical properties of the collecting junction. The conduction band offset ensures that a high surface recombination velocity of the front floating junction does not greatly increase the

leakage current of the collecting junction. Injection of carriers from the base into the emitter is negligible compared to injection from the emitter into the base. The result is that the front surface will not "sink" the injected carriers from the collecting junction. The injected carriers are characterized as the dark diode leakage current. Because the collecting junction's injected carriers are prevented from reaching the front surface, the leakage current and thus the open circuit voltage, are maintained.

Three Dimensional Analysis

The optimal layer thicknesses have been determined by the one dimensional analysis performed using PC-1D. The next procedure towards optimizing the floating junction solar cell is to determine the geometry of the contact grid and the collecting junction. As in any solar cell grid design, there are trade-offs between series resistance losses and shading losses. In the case of the floating junction solar cell, there is no front grid pattern blocking incoming photons from entering the solar cell.

A loss similar to a grid shading loss can occur for photons absorbed far from the collecting junction. This can occur when a photon is absorbed in a region near a base contact. As shown in Figure 12, when the width (b) of the base contacting region is on the order of several diffusion lengths or more, the majority of photogenerated carriers in the base channel region will recombine before diffusing to the collecting junction. Similarly, minority carriers in this region that have been injected across the floating junction will also recombine. This can be considered the base channel recombination loss. The fraction of base channel area to total cell area will present a loss to the cell that is nearly equivalent to a grid shading loss for a conventional solar cell. However, this loss can be eliminated by minimizing the width of the base channel. If the base channel width approaches a minority carrier diffusion length, then all photogenerated/injected carriers near the channel should be collected by the back junction. This will make the short circuit current independent of the total area of base channels and thus the base channel recombination loss or "effective grid shading" will approach zero. An analog of this effect for a conventional solar cell cannot be achieved by minimizing front grid widths because the grid line actually blocks photons from entering the cell (grid shading is proportional to the total grid area).

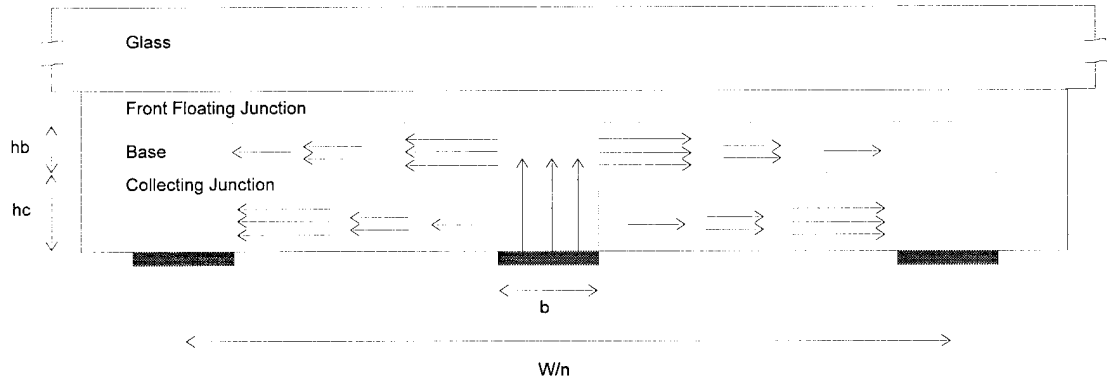


Figure 12. Relevant geometries for grid optimization.

A compromise can be made for a practical floating junction solar cell, so that a significant fraction of the base channel region will contribute to the collected current without requiring

minimum feature sizes on the order of a diffusion length. This will be desirable when fabricating many large area cells, so that yields will remain high. For example, a floating junction solar cell with N base channels, 10 μm wide, would produce a short circuit current loss due to "effective grid shading" approximately 50-60% less than the loss for a conventional solar cell with N front grids 10 μm wide.

The relevant power losses that are to be computed in the following analysis are the base channel recombination loss discussed above, and the resistive loss due to the total base channel resistance, base region and collector. The contact resistances will be considered negligible for the geometries considered.

The resistive losses are caused by Joule heating of the individual current paths in the solar cell. The calculation assumes that current flows as in Figure 12. The Joule heating loss caused by a current carrying element can be expressed as the volume integral:

$$P = \int_V \rho J^2 dV$$

The following expressions represent the resistive losses in the base channel, the base and the collecting junction respectively. Their sum represents the total Joule heating losses for this solar cell model.

$$P_{channel} = \frac{(I_m T)^2 \rho_b h_c}{Wbn} \qquad P_{base} = \frac{(I_m T)^2 \rho_b}{12 h_b n^2}$$

$$P_{collector} = \frac{(I_m T)^2 \rho_c}{12 h_c n^2}$$

where,

W^2 = area of solar cell

b = width of channel to base region

n = number of base channels

h_b = thickness of base region

h_c = thickness of collector region

ρ_b = base resistivity

ρ_c = collector resistivity

T = fraction of active area to total cell area

I_m = current (Amperes)

Thus the total available power for the floating junction solar cell is:

$$P_{total} = P_{theoretical} - P_{channel} - P_{collector} - P_{base}$$

A Microsoft Excel spreadsheet was developed to simultaneously minimize the resistive and effective transparency losses for a floating junction solar cell. Dimensions and losses for a 4x4 cm^2 floating junction solar cell are listed below in Table 5.

The projected efficiency is calculated assuming a starting efficiency calculated by PC-1D. Typical efficiencies for production GaAs cells are 18%-20% (AM0, 1X).

Table 5. Optimal geometry for floating junction cell.

number of base channels	width of base channels	transparency	percent losses	projected efficiency
80	10μm	98.4%	2.64%	21.9%

4.4 Task 4. Demonstrate the technology to accomplish sufficient ohmic contact to n- and p-type AlGaAs in a single contacting process.

The motivation to simultaneously metallize the base and collector contacts is for future manufacturing considerations. Although this task is not expected to actually enhance the performance of the solar cell, it should provide a cost savings for the manufacturing process. The requirements for the metallization are:

- Low contact resistivity (i.e. contact resistivity is comparable to standard n- and p-type contacts)
- Contacts must be highly reliable and stable
- Contact formation may not degrade the performance of the device.

Standard GaAs technologies generally use the Au-Ge-Ni system for n-type contacts. Many GaAs solar cell designers use a Au-Zn or Au-Cr contact for p-type contacting. These contacts do not introduce a significant voltage drop during one sun operation; the contact resistance is negligible compared to the total series resistance of the cell. The conventional contacting sequence requires two different patterning and evaporation steps, which for standard solar cell structures is unavoidable. The all back contact floating junction design provides access to both the n- and p-type material from the back, thus contacting both regions in one step is possible. To accomplish this, a metallization scheme that can provide sufficient conductance for both n- and p-type AlGaAs/GaAs systems is necessary.

Recent developments in high temperature stable contacts demonstrate ohmic contact to both n- and p-type GaAs. PIRLING, ET AL report a high temperature stable contact system based on Pd/In/Pd that can be used on n- and p-type GaAs. Achieving ohmic contact using this system requires a high temperature annealing step approaching 600 °C. Specific contact resistivities of $5x10^{-5}$ Ω-cm^2 and $1x10^{-5}$ Ω-cm^2 are reported for n- and p-type GaAs respectively.

AstroPower has determined that this contact system is capable of providing ohmic contact to n- and p- type $Al_{0.5}Ga_{0.5}As$/GaAs. Contacts were electron beam deposited on n- and p-type material with doping densities of approximately 10^{18} cm^{-3} and 10^{19} cm^{-3} respectively. The contact structure is as follows: Pd(24nm); In(14nm) and Pd(24nm). The contacts were then annealed in forming gas for 20 seconds at 575 °C.

Results

The Pd/In/Pd contact system demonstrated linear current-voltage characteristics on both GaAs and $Al_{0.5}Ga_{0.5}As$. No physical degradation of the contact or semiconductor was evident after the annealing procedure. A modified three-terminal contact resistance measurement was used to estimate the specific contact resistivity of the contact.

Specific contact resistivities of 0.01 and 0.04 Ω-cm^2 were calculated for n- and p-type $Al_{0.5}Ga_{0.5}As$ respectively. However, we believe these measurements are at least one order of magnitude too high. This is because the measurement does not take into account that the effective contact area can be much smaller than the actual contact area. This effective area is defined as the transfer length by [SCHRODER]:

$$L_T = \sqrt{\frac{\rho_c}{\rho_s}}$$

where ρ_c is the specific contact resistance and ρ_s is the semiconductor sheet resistance. Using the specific contact resistivities reported by PIRLING ET AL, a transfer length of 5-10 μm can be approximated using the equation above. A 400 μm contact length was used in this experiment to simplify probing. This suggests that the actual specific contact resistance for these layers is between one and two orders of magnitude lower than the measured values. This compensated value indicates that the Pd/In/Pd contact system would provide a low resistivity ohmic contact to n- and p-type AlGaAs/GaAs solar cells operating under one sun intensity. Further investigations would include the use of a four or six terminal Kelvin test structure for more accurate measurements.

4.5 Task 5. Demonstrate the feasibility of the floating junction solar cell by building a prototype device and characterizing the performance.

Thirteen floating junction solar cells were fabricated during the Phase I effort. Solar cells were fabricated following the general process sequence outlined in Section 4.2. The results of the highest efficiency floating junction GaAs solar cell fabricated during the Phase I program are shown in Figure 13. The cell was tested using AstroPower's solar simulator with a xenon arc lamp, calibrated with a GaAs standard. Figure 14 displays the internal and external quantum efficiency of the floating junction structure. These results are a clear demonstration of the potential performance of the GaAs floating junction solar cell.

Cell # G14408(450)

Area:	1 cm^2
Simulation:	AM0, 1X
Open Circuit Voltage:	880 mV
Short Circuit Current:	26.77 mA
Fill Factor:	62.8 %
Maximum Power:	14.8 mW
Efficiency:	11.0%

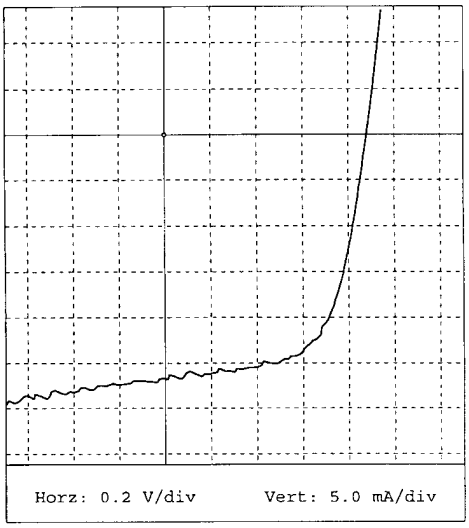


Figure 13. Illuminated IV characteristics of floating junction GaAs solar cell.

Figure 15 shows the front and back surfaces of two 1 cm^2 floating junction solar cells. The cell on the right is the 11% efficient cell described above. Figure 15 (a) is a photograph of the front surface of the cell and the back surface of the cell is shown in Figure 15 (b). The cell is electrostatically bonded to high temperature E10050 glass and the GaAs is approximately 3 micrometers thick. An interesting physical feature of the solar cell is that the front surface contains absolutely no metallization; all metallization is located at the back of the device.

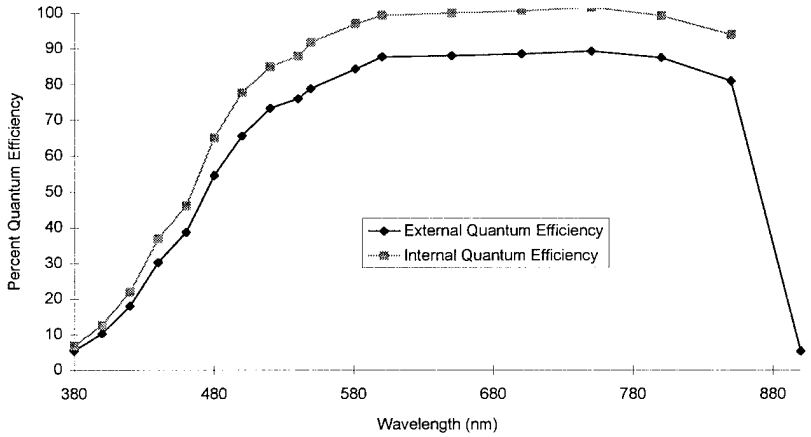
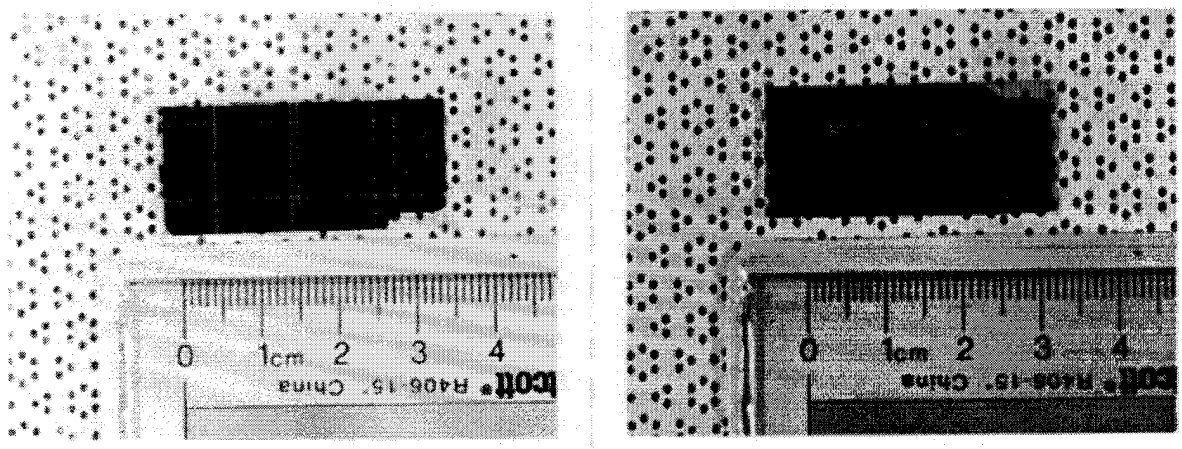


Figure 14. Quantum efficiency measurements of floating junction GaAs solar cell #G14408(450).



(a) front *(b) back*

Figure 15. Front (a) and back (b) surfaces of two 1cm^2 floating junction solar cells.

Discussion

The Phase I effort has demonstrated the feasibility of the floating junction GaAs structure as a potential high efficiency space solar cell. The results indicate that the device is performing as predicted; carriers generated in the vicinity of both the floating and collecting junction contribute to the short circuit current. This is apparent from the quantum efficiency data and short circuit current density. The quantum efficiency reveals that light strongly absorbed between the surface and the front floating junction does contribute to the short circuit current. For example, light of 500 nm wavelength has an absorption coefficient of approximately $7x10^4cm^{-1}$ and thus over 80% of the available photons at this wavelength are absorbed in the emitter. Based on the quantum efficiency data, the solar cell is converting nearly 80% of the available photons into current at this wavelength. If this were not the case, the quantum efficiency at 500 nm would be less than 20%.

The data indicates that there are two dominating losses for the solar cell resulting in a low open circuit voltage and moderate short circuit current. These losses include a low shunt resistance and a poor blue wavelength response. The low shunt resistance of approximately 260 Ω is attributed to processing, specifically the diffusion barrier. During the Phase I program, it was found that the shunt resistance was related to the thickness, deposition parameters and subsequent processing of the $Si_xO_yN_z$ diffusion barrier. Initial floating junction solar cells exhibited shunt resistances of approximately 100 Ω-cm^2 or less. Speculation into the nature of the high shunt conductance included the possibility that, some or all, of the barrier was allowing an extremely thin p-type region to diffuse underneath the barrier. Thus the alloyed n-contact would not be isolated from the diffused p-region. The situation improved by implementing a thick, dense $Si_xO_yN_z$ layer deposited at an increased PECVD chamber temperature. However, further improvements are necessary to increase the shunt resistance of the solar cell. The use of multiple layers of $SiO_2/Si_xO_yN_z$ may decrease the pinhole density of the barrier layer that is associated with a PECVD oxide/nitride deposition. By eliminating the shunt resistance problem, we anticipate that the open circuit voltage will increase.

The cause of the poor blue response is associated with non-optimal layer thicknesses, and thus is not associated with the floating junction design or fabrication process. Processing a standard GaAs control cell (with a supporting substrate and no glass superstrate) reveals that the poor blue response exists prior to any high temperature processing. The growth conditions for the standard cell and the floating junction cell were identical. The internal quantum efficiency curve of the standard control is depicted in Figure 16. By using optimal layer thicknesses and growth techniques, an increase in blue response is anticipated for the floating junction GaAs solar cell.

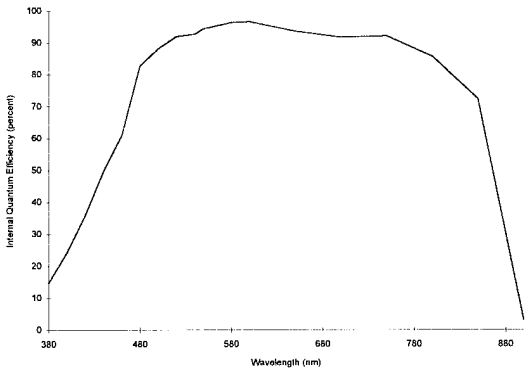


Figure 16. Quantum efficiency for a standard top/bottom LPE grown GaAs p/n solar cell.

5.0 SUMMARY AND CONCLUSIONS

AstroPower has demonstrated the feasibility of the ultra-thin, floating junction GaAs solar cell. Each of the Phase I objectives outlined in the Phase I proposal was achieved. The key result is the fabrication of a 3 μm thick floating junction GaAs solar cell with an AM0, 1X efficiency of 11%. Additionally, the development of the electrostatic bonding process of GaAs to a CTE matched, high temperature glass resulted in 3 μm thick GaAs laminates capable of surviving processing temperatures of up to 700 °C. This ensures stability of the electrostatically bonded GaAs solar cell throughout the process sequence. Conventional semiconductor device modeling predicts an AM0, 1X efficiency of 21.9% for the floating junction GaAs solar cell. In addition, proper design of the floating junction solar cell exhibits a potential radiation resistance that surpasses conventional GaAs solar cell designs.

We conclude that the floating junction GaAs solar cell design proposed for space applications is not only feasible, but manufacturable. The major technical objectives of the Phase II are indicated as follows:

1. To continue development of the electrostatically bonded floating junction GaAs solar cell, including the high temperature process sequence.
2. To optimize the device for maximum current collection and passivation benefits.
3. To deliver high performance, high specific power, floating junction GaAs solar cells for testing and evaluation to demonstrate the potential of this technology.

The specific goals of the Phase II program can be summarized as:

- Obtain device layers for a high performance floating junction GaAs solar cell
- Optimize the electrostatic bond process and diffusion of the collecting junction
- Solar cell characterization
- Demonstrate light trapping in floating junction GaAs solar cell
- Space qualify the high temperature glass
- Collaborate with a laboratory that will conduct radiation testing on floating junction GaAs solar cell prototypes
- Increase solar cell area
- Develop solar cell and fabrication process for manufacturing

The technology developed during the Phase I and II programs can be applied to other GaAs electronic devices and circuits. The benefits of high temperature processing of electrostatically bonded GaAs laminates may be transfered not only to other solar cell designs, but to the microelectronics industry. A thermally conductive, high temperature substrate can be electrostatically bonded to thin GaAs layers. After substrate removal, ultra-thin devices and circuitry may be fabricated on the thermally conductive substrate using the high temperature GaAs/laminate processing techniques developed during this program. High powered, ultra-thin GaAs electronic components and circuits can operate efficiently and reliably, due to increased heat dissipation from the ultra-thin device layers, when compared with similar devices on GaAs or Ge substrate. This device technology can be applied to high operating temperature electronic components such as microwave circuitry, surface emitting lasers and concentrator cells.

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13. ABSTRACT *(Maximum 200 words)*

AstroPower has demonstrated the feasibility of a lightweight, high efficiency GaAs solar cell that will have superior performance characteristics compared to conventional GaAs solar cells in the space environment. The solar cell design consists of a front floating junction that is coupled to a back collecting junction through the injection of minority carriers across a thin base. Performance benefits are enabled by incorporating an all back contact design with the electrostatic bonding technique and the use of multiple active junctions. By using the proper geometrical and electrical considerations, losses associated with grid shading and low energy radiation damage will be minimized. The key results of the Phase I program include demonstration of an 11% efficient (AMO, 1X), 1cm^2 floating junction GaAs solar cell and a 3 μm thick GaAs layer electrostatically bonded to high temperature glass capable of surviving process temperatures up to 700 °C. This ensures stability of the laminate throughout the process sequence and enables numerous potential applications for thin GaAs semiconductor devices. Continuation of process development in Phase II is anticipated to produce, when fully optimized, a radiation resistant solar cell which has been modeled to have an efficiency of 21.9%.

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